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## PROBABILITY CHARACTERISTICS OF THE RELIABILITY OF THE TRANSITIONAL STATES OF A SEMICONDUCTOR TEMPERATURE CONVERTER AT A JOINT WORK BY INTEGRAL MICROCHARTS

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Annotation: The probabilistic characteristics of the reliability of transition states of a semiconductor converter when working together with integrated circuits are considered. The probability of an effective transition of an integrated circuit that functions with a semiconductor converter from a state of logical zero to a state of logical unit is established, and the corresponding probability equations are obtained for a sufficient signal duration and pause.

**Keywords**: reliability, transition states, semiconductor converter, logical unit, effective zone, transition probability.

### I. INTRODUCTION

During the operation of information-measuring devices and systems failures occur, which can be sudden and gradual. Sudden failures fall into the category of random events. The physical nature of sudden failures is due to the concentration of loads that cause the corresponding internal damage in the form of an interruption or short circuit of the windings, breakage of parts, and others.

The failure of any element and information device, in particular, a measuring transducer of physical quantities, can be determined by the action of the following factors: structural imperfections of the source materials of the product, due to the presence of impurities, dislocations and concentration gradients; external influences - thermal mechanical and electrical loads [1,2].

Failures of information devices and systems are random events. However, the reasons for the occurrence of failure are associated with certain physical and physico-chemical processes occurring in materials and structures during operation. The choice of the approach to the determination of reliability by the methods of the physics of failure is determined by the assumption that chemical reactions and physical processes occurring on the surface and inside the measuring device cause deterioration of its electrical characteristics and, as a result, catastrophic and parametric failures.

### **II. RESULTS AND DISCUSSION**

Consider the probabilistic characteristics of the reliability of the transition states of a semiconductor transducer of humidity of dispersed media with the joint operation of integrated circuits. The reliability of the integrated measuring circuits of semiconductor transducers of physical quantities in terms of the absence of parametric faults is determined from the value of the margin of functional (static and dynamic) stability. Static stability is understood to mean signal transmission by logic circuits, in which the transition of single signals to zero and zero to single signals, which is not provided by the logical functions, does not occur.

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The dynamic stability of signal transmission by logic elements should be understood as the preservation of a sufficient signal duration and a sufficient pause duration to ensure a transition from a state of logical zero to a state of logical one and vice versa. Functionally stable logical elements are characterized by two stable sections (Fig.1).

If we draw straight lines parallel to the ordinate axis through points A, B, C and D, we obtain boundary lines characterizing the stable operation zones of the logic element, which is associated with the effective transition of electrons from the valence band to the conduction band in a semiconductor, functioning as a converter. The input signal in zone I is characterized by astable initial value, and for zone III, a stable operating state.



Fig.1. Stable transition zones of a logic element of a semiconductor converter

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For zone I  

$$\pm U = U_n + U_0,$$
(1)

where U- possible fluctuations in the value of the input signal;  $U_n$ - mixing of the input signal due to interference;  $U_0$  is the mixing of the input signal of the semiconductor converter due to the influence of temperature.

For zone II  

$$\pm U' = U'_0 + K_2 \sigma_a,$$
(2)

where  $U'_0$  - displacement characteristics caused by changes in temperature;  $\sigma_a$ -the mean square deviation of the values corresponding to the given section of the characteristic. It can be determined from the ratio  $\sigma_a = m\overline{U}$ .

With modern technology  $m = 0.08 \div 0.15$ ,  $K_2 \ge 3.0$ . For zone III  $\pm U'' = \Delta U$ . (3)

As the most important static parameters, we give four values of voltages. Four voltagevalues define the display limits of the variables (0 and 1) at the output and input of the element. For normal operation of the element, it is required that the voltage representing the logical unit is sufficiently high, and the voltage displaying 0 be sufficiently low. These requirements are set by parameters  $U_{inp.1min}$  and  $U_{inp.0max}$ . The input

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voltage of a logic element is the output voltage of the previous one (signal source). The levels guaranteed at the output of the logic element when the permissible load conditions are observed are set by parameters,  $U_{outp.1.min}$  and  $U_{outp.0.max}$ . The output levels are slightly better than the input levels, which provides a certain noise immunity of the element. For level U, negative interference is dangerous, reducing it, and the permissible static interference [4]

$$U_{nom}^{-} = U_{outp.1\min}^{-} - U_{inp.1\min}^{-}.$$

For level  $U_0$ , positive interference is dangerous, with acceptable static interference

 $U_{nom}^{+} = U_{outp.0.\,\text{max}} - U_{inp.0\,\text{max}}$ .

To perform a stable signal transmission through the logic element of the measuring transducer, it is necessary to fulfill the condition that the I and III bands do not overlap with a spread of  $\pm U$  and  $\pm U'$  to the band II, that is, the stability of the logic circuit is characterized by the stability margin for the input voltage level «0»:

$$S_{0} = \left| U_{inp.0 \max} - U_{inp.0} \right| \ge 0$$
  
and for input voltage level «1»: (4)

$$S_1 = |U_{inp.1} - U_{inp.1\min}| \ge 0$$
,

where  $U_{inp,0}$ ,  $U_{inp,1}$ - the magnitude of the input voltage level «0» and «1», respectively;

 $U_{inp.0\,\mathrm{max}}$  - the maximum allowed input level of the signal at which the circuit is still in a state of logical

one.

Thus, the magnitude of the stability margin of integrated circuits, taking into account the variation of parameters, is determined for the level «0»:

$$S_{0} = \left\{ U_{inp.0 \max} - \Delta U_{inp.0 \max} \left| - \left| \Delta U_{inp.0} + U_{inp.0} \right| \right\}$$
(5)

and for input voltage level «1»

$$S_{1} = \{ \left| U_{\text{inp.1}} - \Delta U_{\text{inp.1}} \right| - \left| U_{inp.1 \min} + \Delta U_{inp.1 \min} \right| \} \ge 0$$
(6)

Values  $U_{inp.0}$ ,  $U_{inp.1}$ ,  $U_{inp.0 \max}$ ,  $U_{inp.1\min}$  are independent random events and their density distribution functions can be represented on a common abscissa axis in the form of four normalized curves or, using the composition rules, one can obtain two normalized curves (Fig. 2).



Fig.2. Stable transition zones from the state of logical zero in the state of logical'unit of functionally logical elements

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The probability of an effective transition of an integrated circuit of a semiconductor converter from a state of logical zero in a state of logical one when a signal is applied to the input  $U_{inp.0}$  and fulfilling the condition,  $S_0 \ge 0$  determined by the expression:

$$P_{\beta_{1}}(0 < S < \infty) = 1 - \frac{1}{\sqrt{2\pi\sigma_{S_{0}}}} \cdot \int_{-\infty}^{0} \exp\left[-\frac{(U_{inp.} - S_{0})^{2}}{2\sigma_{S_{0}}^{2}}\right] dU_{inp},$$
(7)

where  $\sigma_{s_0} = \sqrt{\sigma_0^2 + \sigma_z^2}$  - the average quadratic deviation;  $\sigma_z$  - the average quadratic deviation of the value  $\overline{U}_{inp.0 \text{ max}}$ ;  $\overline{U}_{inp.0}$ -mathematical expectation of the value  $U_{inp.0}$ .

Expressing the integral through the Laplace function and passing to other limits of integration, we get

$$P_{\beta_{1}} = 0.5 + F \left[ \frac{S_{0}}{\sigma_{S_{0}}} \right] = 0.5 + F \left[ \frac{\overline{U}_{inp.\,\text{max}} - \overline{U}_{inp.0}}{\sigma_{S_{0}}} \right]$$
(8)

Similarly, the probability of correct operation of the circuit when a voltage is applied to the input  $U_{inp,1}$ , characterizing the transition of the element from the state of a logical unit to a state of logical zero and the condition  $S_1 > 0$ , determined by the expression

$$P_{\beta_{2}}(0 < S_{1} < \infty) = 1 - \frac{1}{\sqrt{2\pi\sigma_{S_{1}}}} \int_{-\infty}^{0} exp \left[ -\frac{(U_{sx} - \overline{S}_{1})^{2}}{2\sigma_{S_{1}}} \right] \cdot dU_{inp.1}$$

$$P_{\beta_{2}} = 0,5 + F\left[\frac{\overline{S}_{1}}{\sigma_{S_{1}}}\right] + F\left[\frac{|\overline{U}_{inp.1\min} - \overline{U}_{inp.1}|}{\sigma_{S_{1}}}\right], \quad (10)$$

$$(9)$$

or

where  $\sigma_{s_1} = \sqrt{\sigma_1^2 + \sigma_s^2}$  - standard quadratic deviation, and  $\sigma_1$ - standard quadratic deviation of value  $\overline{U}_{inp.1\min}$ ;  $\overline{U}_{inp.1\min}$  - mathematical expectation of the value  $U_{inp.1}$ .

(11)

We will evaluate the parametric reliability with dynamic stability of the logic integrated circuit of the measuring transducer. The duration of the working signal is selected on the basis of its minimum duration necessary for reliable triggering of the circuit:

$$\tau_H = k \tau_{H \min}$$

where k – coefficient actuation ( $k = 1,5 \div 4,0$ ).

The magnitude of the decrease in the duration of the signal  $(\Delta \tau_n)$  with the passage of the signal through the *n*-1 element is defined as

$$\Delta \tau_{\mu} = \tau_{\mu} (n-1)^{-\tau_{un}},$$

where  $\tau_{un}$  and  $\tau_{u(n-1)}$ - pulse duration on *n* and (*n*-1) elements, respectively.

The magnitude of the decrease in the duration of the pause when the signal passes through the n element is defined as

 $\Delta \tau_{n\mu} = \tau_n (n-1),$ 

where  $\tau_{u(n-1)}$  and  $\tau_{un}$  - duration of pauses (n - 1) and n circuits, respectively.

The scheme will have dynamic stability if the condition

$$S_{\partial u} = \left| \overline{\tau}_{u} - \tau_{u \min} \right| \ge 0,$$

$$S_{\partial u} = \left| \overline{\tau}_{np} - \tau_{n \min} \right| \ge 0,$$
(12)

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where  $\tau_{np}$ -mathematical expectation length of pause;  $\tau_n$ -mathematical expectation of value  $\tau_{np}$ .

Taking into account (12), the probabilities of correct operation of the *n*-circuit with sufficient signal duration and pause are determined respectively by the expressions:

$$P_{\beta_{3}}\left(0 < S_{\partial u} < \infty\right) = 1 - \frac{1}{\sqrt{2\pi\sigma_{s}}} \int_{-\infty}^{\sigma} exp - \left\{\frac{\left[\tau_{u} - \left(\bar{\tau}_{u} - \tau_{u\min}\right)^{2}\right]}{2\sigma_{s}^{2}}\right\} d\tau_{u},$$

$$P_{\beta_{3}} = 0.5 + F\left[\frac{\bar{S}_{\partial u}}{\sigma_{s}}\right] = 0.5 + F\left[\frac{\bar{\tau} - \tau_{u\min}}{\sigma_{s}}\right],$$
(13)

or

$$P_{\beta_{4}}\left(0 < S_{\partial u} < \infty\right) = 1 - \frac{1}{\sqrt{2\pi\sigma_{S}}} \int_{-\infty}^{0} exp\left\{-\frac{\left[\tau_{n} - \left(\overline{\tau}_{n} - \tau_{n\min}\right)\right]}{2\sigma_{z}^{2}}\right\}} d\tau_{n}$$

$$P_{\beta_{4}} = 0,5 + F\left[\frac{\overline{S}_{\partial u}}{\sigma_{z}}\right] = 0,5 + F\left[\frac{\overline{\tau}_{np} - \tau_{n\min}}{\sigma_{z}}\right].$$
(15)

 $(1\Lambda)$ 

#### **III. CONCLUSION**

Thus, from equation (14) and (16) it can be seen that the probability of operation of an integrated circuit, which functions together with a semiconductor converter, depends on the value of the function F(x), since with increasing its value the probability of operation of the integrated circuit increases, since this the process is accompanied by a sufficient signal duration and a pause with the same rams transition error. Consequently, with an increase in the mean-square error of the transition, the probability of operation of an integrated circuit, which works with a semiconductor converter, is significantly reduced, which is characterized by the transition of electrons with high probability from the valence band to the conduction band.

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